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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,908	07/24/2006	Akihiro Goto	1032404-000154	1812

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
01/26/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/586,908	GOTO ET AL.	
	Examiner	Art Unit	
	NGHIA M. DOAN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Applicant Amendment filed on 10/21/2008. Claims 11-20 remain pending. Claims 1-10 have been canceled.

Claims 11 and 12 have been withdrawn.

Claims 13, 17, and 18 have been amended.

The amended drawing is accepted.

The amended specification is accepted.

Response to Arguments

2. Applicant's arguments, filed 10/21/2008, with respect to Election/Restriction required have been fully considered and are persuasive. The Election/Restriction required has been withdrawn. Therefore, claims 11 and 12 now is examined.

3. Applicant's arguments with respect to claim 13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 11-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims 11-13 appear no practical application and no tangible result after analyzing step being performed that is useful nor transformed thing to another state. There nothing recites any utility or result or outcome

that is practice the claim invention. The “analyzing” is deficiencies to omit the utility to practical the claim invention. (Note: such semiconductor chip being transformed to other state based on "analyzing result” that is practical and useful in real world application.

6. Claims 14-20 are also rejected because are depended directly or indirectly from claim 13.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 11 and 12 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. As respect to claims 11 and 12, recited the limitation "fluctuation arrangement” which renders the claim indefinite because it is unclear what “fluctuation” means and roles and how to specify/evaluate “fluctuation” in the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eka et al., (US Pat. 6,357,036) in view of Bon et al., (US Pub. 20010044660) (see entire documents).

11. With respect to claims 11-13, Eka teaches a bond tool utility software package which extracts bond pad (interposer) location data from a semiconductor chip design and retrieves bonding connection data to generate a bonding diagram for the semiconductor assembly, the software package including a data file comprising a silicon bond pad layout ('036, fig. 1, [220]), which represents the location (position) of individual pads within a semiconductor device as determined after initial circuit design, a pad should be located within a certain distance relationship between the edge of the chip over which the wire bond is formed ('036, col. 4, ll. 7-13) . Both layout extraction utilities 215 and 235 may also be fed with Net List/Pin Assignment data 240. Net List/Pin Assignment data 240 may comprise the connectivity between various pins on the semiconductor device and the corresponding bond pads. Hence it may be necessary to include such data in order to determine the general bonding pattern (bond wire connection terminal position of the interposer) ('036, col. 3, ll. 48-65). From the extracted layout data and netlist/pin assignment data, a database may be created representing layer coordinates and pin assignments and may include location data for each pad, as well as the pad assignment, its connectivity to particular pins and those pin assignments. From such data, a wire bonding diagram may be generated (creates simulation design first data) ('036, col. 4, line 26 - col. 5, line 4).

Package drawing 270 data may be fed to autocad program 265 which may be modified by a C-program utility to generate package information 285. Package information 285 may comprise that portion of package drawing 270 which illustrates the location of leads 130, 140, 150, and 160. Package information 285 and database 250 may then be fed to C-program utility 260. C-program utility 260 receives pad layer coordinates and pin assignment from database 250 and package information data 285 and feed all data through design rule check utility 255 (creates simulation design second data) ('036, col. 5, ll. 5-17).

Design rule check utility 255 may comprise a C-program which will check angles and distances of leads from the package leads to silicon pads (measuring a design rule) (col. 5, ll. 17-20); and

Determining (analyzing) whether a rule violation has occurred (Note: design rule includes a tolerance). If a bonding rule violation has occurred, C-program utility 260 may do one of two things. First, a user may be alerted of the violation and allowed the opportunity to correct the violation manually. The user may then utilize AUTOCAD drafting software to move a silicon pad to correct the design rule violation. The revised AUTOCAD file may then be fed back through C-program utility and design rule check utility to determine whether the revised design contains and bond rule errors. In a second technique, C-program utility may be programmed to automatically correct for bonding rule error by relocating pads on the silicon design. In either instance, once the bonding diagram meets all design rule criteria, an AUTOCAD file 275 may be produced comprising the revised bonding diagram. AUTOCAD file 275 may be fed to AUTOCAD

utility 280, which may comprise custom code, to output a bonding diagram 285. AutoCad utility 280 may also output corrected pad location data to circuit design program interface 290. Circuit design program interface 290 may comprise a C-program utility patch to one of a number of circuit design programs offered by a number of providers (e.g., Cadence, Avant!, or the like). Circuit design program interface 290 may alter the data file for the circuit design to correct the silicon bond pay layout in view of any design rule violations previously detected ('036, col. 5, ll. 21-46).

Eka does not teach the occurrence of fluctuation (deviation) in an arrangement position of a semiconductor chip on bond pad.

Bon discloses a design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer, the design support apparatus comprising: a creating unit that creates simulated design data simulating occurrence of fluctuation (irregular or variable) in an arrangement position of a semiconductor chip on an interposer (bond pad) (irregular circuit position or variable chip position during attachment to the lead frame) on bonder for attaching connecting bonds on the IC bond pad) ('660, the abstract, paras. [0006] [0021]) and occurrence of fluctuation (variable) in bond wire connection terminal positions of the interposer (bond pad) ('102, the abstract, para. [0048] [0049] [0067] [0072]).

It would have been obvious to one of ordinary skill in the art to combine Eka and Bon to provide a fast, reliable, and flexible system and method to reduce set-up time, reducing errors during creation and retrieval of bonding program, compensate for machine variability that system and method should spearhead solution toward the goals

of improved product yield, reliability, and flexible enough to be applied for different IC product families without investment in new equipment ('660, para. [0020])

12. With respect to claim 14, Eka and Bon teach wherein the design data of the semiconductor package includes shape (geometry) of the interposer, shape of the semiconductor chip, an arrangement position (locations/coordinates) of the semiconductor chip on the interposer, shape of the bond wires that connect the semiconductor chip and the interposer, and arrangement positions (locations/coordinates) of the bond wires that connect the semiconductor chip and the interposer ('660, para. [0022] [0027] [0067] [0070] [0071] [0082] [00129]).

13. With respect to claim 15, Eka and Bon teach wherein the first data creating unit creates semiconductor chip simulated arrangement data obtained by arranging, with respect to the arrangement position of the semiconductor chip on the interposer in the design data of the semiconductor package, the semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in an in-plane direction or a rotation direction on a semiconductor chip arrangement surface of the interposer or fluctuation in inclination of the semiconductor chip in a thickness direction of the interposer is simulated ('660, paras. [0011] [0023] [0029] [0030] [0049]).

14. With respect to claim 16, Eka and Bon teach wherein the measuring unit measures clearance between the bond wires and clearance between the bond wires and the semiconductor chip as the design rule ('036, col.4, ll. 7-13 and col. 5, ll. 17-21).

15. With respect to claim 17, Eka and Bon teach wherein the analyzing unit analyzes a tolerance of fluctuation in an arrangement position of the semiconductor ship on the interposer that satisfies the design rule ('036, col. 4, ll. 7-13, col. 5, ll. 21-30).

16. With respect to claim 18, Eka and Bon teach wherein the analyzing unit analyzes a tolerance of fluctuation in bond wire connection terminal positions of the interposer that satisfies the design rule ('036, col. 4, ll. 7-13, col. 5, ll. 31-37).

17. With respect to claim 19, Eka and Bon teach comprising a storing unit (database) that stores therein the measurement result ('036, col. 4, ll. 34-65 and col. 5, ll.1-4).

18. With respect to claim 20, Eka and Bon teach comprising a storing unit that stores therein analysis result obtained by the analyzing unit ('036, col. 5, ll. 21-46).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGHIA M. DOAN whose telephone number is (571)272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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